DEBASHISH NANDI

PhD Scholar (PMRF), IIT Kanpur

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EDUCATION

2022-Current — **Ph.D.: Microelectronics And VLSI**
Indian Institute of Technology Kanpur - Kanpur, UP
Coursework Details: Annexed.
CGPA: **9.90**/10

2013 -2017 — **B.Tech.: Electronics and Communication Engineering**
National Institute of Technology, Durgapur - Durgapur, WB
CGPA: **9.47**/10 (in absolute scale); Rank: **10** (in university)

2013 — **Higher Secondary: P-C-M-B**
Jitpur High School - Alipurduar, WB
Grade: **92.8%**; Board: WBCHSC; Rank: **9** (in State)

2011 — **Secondary: General**
Railway Higher Secondary School - Alipurduar, WB
Grade: **90.25%**; Board: WBBSE; Rank: within Top 100 (in State)

WORK EXPERIENCE

2017 -2021 — **Asst. Manager (E&C)**
Larsen and Toubro Limited, Faridabad, HR, India

Key Responsibilities:
1. End to end design integration of Railway Telecom subsystems namely SDH-PDH, WAN, GSM-R, Master Clock System, EPABX, DTS, PAS, PIDS for DFCCIL, Indian Railways mainline (new & modification), Metro Projects in India and abroad, as part of EDRC (Engineering Design and Research Centre).
2. Integration of Telecom systems with Signalling Works, E&M works, Track works, Train Management System, Electronic Interlocking.
3. Planning, Cost Controlling of Signalling and Telecom works for DFCCIL CTP-14 (Rewari-Dadri) Project valued INR 3799 Cr.
4. Interface Management for S&T works with stakeholders (mainly GOI, JICA) of the WDFC CTP-14 Project.
Key Skills Acquired: Telecom System Design, Project Management, RAMS, System Integration

INTERNSHIPS AND TRAININGS

2017 — **Graduate Engineer Trainee**
Competency Development Centre, Kanchipuram, TN

Undergone 1-month comprehensive training in Railways construction including design and EPC contract management. Trained in P-way, OHE, PSI, Signalling and Telecom system Design and Construction. Secured 3rd rank in the final evaluation among 24 students.
Key Skills Acquired: Basics of Railways construction, EPC Contract management, FIDIC.

2016 — **Research Intern**
Indian Institute of Technology Guwahati, AS

Worked under guidance of **Dr. Gaurav Trivedi** (Associate Professor, EE) on Atomistic Simulations in 'Virtual Nanolab ATK tool' for 2D materials like Silecene, Germanene, Stanene etc. Investigated Bandgap generation in these materials by studying their band structures, introducing various defects namely Stone Wales, Single vacancy etc. Also studied their terminal characteristics by simulating various device structures.

Key Skills Acquired: 2D simulations on ATK tools like Virtual Nanolab, Research paper writing, Conference presentation.

2015

Trainee Intern

Hewlett-Packard Education Services, Kolkata, WB

Undergone 1-month hands-on training in Embedded Systems and Robotics - Basics and Advanced. Have worked on PCB design, PCB integration and made a line following robot as part of the end-project. Secured 2nd rank in the final evaluation among 30+ students.

Key Skills Acquired: Embedded Systems basics, MMI, PCB design.

CO-CURRICULAR ACTIVITIES

1. 2023-2024: IEEE U.P. Section Student Representative, managed a team of 20 students to manage all student activities.
2. 2013-2014: Member of National Service Scheme in NIT Durgapur and taught underprivileged students from nearby villages below class X.
3. 2011: Organized and managed science exhibition in Jitpur High School, Alipurduar, WB.
4. Interests: Teaching, Literature, Badminton, Football, Table Tennis. Snooker.

AWARDS/HONORS

1. 2022: Received Prime Minister's Research Fellowship to pursue PhD in the broad area of Electrical Engineering.
2. 2018-2021: Rated Top Performer in every financial year performance review in Larsen & Toubro.
3. 2013: Chief Minister's (WB) award of excellence (along with a laptop) for securing State Rank-9 in Higher Secondary Examination.
4. 2013: Divisional Railway Manager's (APDJ) award of excellence in Higher Secondary Examination.
5. 2005: State sponsored scholarship (*Vritti*) of excellence in completion of Primary education.

LANGUAGES

Bengali, Hindi: Native Proficiency
English: Full Professional Proficiency
Assamese: Elementary Proficiency

PUBLICATIONS

1. G. Kumar, M. Singh, **D Nandi**, G Trivedi, Bandgap generation in 2D materials, ***IEEE conference Devices for Integrated Circuit (DevIC)***, 2017, doi: 10.1109/DEVIC.2017.8074011
2. C K Dabhi, D Rajasekaran, G Pahwa, **D Nandi**, N Karumuri, S Turuvekere, A Dutta, B Swaminathan, S Srihari, Y S Chauhan, C Hu, "Symmetric BSIM-SOI Part-I: A Compact Model for Dynamically Depleted SOI MOSFETs", ***IEEE Transactions on Electron Devices****, v.71(4) pp. 2284-92, 2024,* doi: 10.1109/TED.2024.3363110
3. C K Dabhi*, **D Nandi***, K Nandan, D Rajasekaran, G Pahwa, N Karumuri, S Turuvekere, A Dutta, B Swaminathan, S Srihari, Y S Chauhan, S Salahuddin, C Hu, "Symmetric BSIM-SOI Part-II: A Compact Model for Partially Depleted SOI MOSFETs", ***IEEE Transactions on Electron Devices,*** *v.71(4) 2293-2300, 2024,* doi: 10.1109/TED.2024.3363117
4. **D. Nandi**, C. K. Dabhi, D. Rajasekharan, N. Karumuri, S. Turuvekere, B. Swaminathan, S. Srihari, A. Dutta, C. Hu and Y. S. Chauhan "Validation of Dynamically Depleted Symmetric BSIM-SOI Compact model for RF SOI T/R Switch Applications", ***IEEE conference on Electron Devices Technology and Manufacturing (EDTM)***, *2024*
5. Y. H. Zarkob, A. Sharma, G. Pahwa, **D. Nandi**, C. Dabhi, V. Kubrak, B. Peddenpohl, M. Tang, C. Hu and Y. S. Chauhan "Compact Modeling and Experimental validation of Reverse Impact Ionization in LDMOS transistors within the BSIM-BULK framework", ***IEEE conference on Electron Devices Technology and Manufacturing (EDTM)***, *2024*

**Equal Contribution first author*

Enclosed: Annexure-1 (PhD Coursework Details & Teaching experience)

ANNEXURE-1

PhD Coursework Details (IIT Kanpur)

S. No.	Subject Code	Subject Name	Semester	Grade	Project/Term Paper
1.	EE-681A	*Compact Modelling* **Instructor:** Prof. Yogesh Singh Chauhan	2021-2022 (II)	A	1. Parameter Extraction of BSIM4 2. Development of Verilog A Code for BULK MOSFET
2.	EE-613A	*High Frequency Analog Circuit Design* **Instructor:** Dr. Imon Mondal	2021-2022 (II)	A	1. Design of LDO. 2. Design of Two-Stage Fully Differential Miller Compensated OPAMP
3.	EE-619A	*VLSI System Design* **Instructor:** Dr. Rik Dey	2021-2022 (II)	A	Design of Multiple Digital Combinational Circuit Blocks and Verilog Implementation in Behavioral, Structural, Data Flow Levels
4.	EE-698N	*Introduction to Flexible Electronics* **Instructor:** Prof. Baquer Mazhari	2021-2022 (II)	A	Role of Carbon Nanotube, applications and its advancement in Flexible Electronics.
5.	EE-614A	*Solid State Devices I* **Instructor**: Prof. Aloke Dutta	2022-2023 (I)	B+	N/A
6.	EE-616A	*Semiconductor Device Modelling* **Instructor**: Dr. Rik Dey	2022-2023 (I)	A*	N/A
7.	EE-698F	*RF Microelectronics* **Instructor:** Prof. Yogesh Singh Chauhan	2022-2023 (I)	A*	Design of Low Noise Amplifier in 2-4GHz Frequency band with GaAs HEMT.
8.	EE-648A	*RF Microelectronics* **Instructor:** Dr. Raghavendra Chowdhury	2022-2023 (II)	A*	1. Analysis of Theory of Small Reflections for CCITLs. 2. Analysis of Async. Coupled Lines in Inhomogeneous Medium.
9.	EE-656A	*RF Microelectronics* **Instructor:** Prof. Nishchal Kumar Verma	2022-2023 (II)	A	Implementation of Self-Optimal Clustering Algorithm.
10.	EE-647A	*Microwave Measurements and Design* **Instructor:** Prof. A R Harish	2023-2024 (I)	A	Multiple RF Characterizations on various Microwave DUTs.

Grading Scheme:

A*	A	B+	B	C+	C	D+	D	E	F	I
10	10	9	8	7	6	5	4	0	0	0

Teaching Experience:

1. NPTEL NOC EE-62: Basic Electronics (Jan'23 to Apr'23)
   Instructor: Prof. Mahesh B Patil (IIT Bombay)
   YouTube Link: NPTEL NOC EE-62 Tutorials

2. MATLAB Workshop at CSJMU (Kanpur University)

3. NPTEL NOC EE-91: Semiconductor Devices and Circuits (Jul'23 to Oct'23)
   Instructor: Prof. Sanjeev Sambandan (IISc Bangaluru)
   YouTube Link: NPTEL NOC EE-91 Tutorials

4. Dept. of ECE, CSJMU (Kanpur University): Comprehensive Circuit Analysis with SPICE (Jan'24 to Mar'24)
   Description: Designed and instructed.
   Course Website Link: Course Website